ABSTRACT OF THE DISCLOSURE

A data processing device has a CPU, a cache memory, a cache control part, and a memory control part accessible to a memory in response to a cache mishit of the cache memory. In having access to a burstable memory in response to a cache mishit, a memory control part generates first information for indicating a burst length of the memory to a cache line length of the cache memory, and it can control a single or plurality of burst operations necessary to obtain a data length meeting the cache line length according to the first information. The cache control part can control the operation of filling data acquired in the single or plurality of burst operations in the cache memory by wraparound according to the first information. Data outputted from the memory does not need to be sorted by an aligner and there is no need to provide the restriction of fixing the top boundary of a data block for burst operations to a start access address. Therefore, waiting time of the CPU until acquiring data in a cache miss can be shortened even when using a memory with a burst length shorter than the cache line length.